WHAT IS CLAIMED IS:

1. A digital PLL device outputting a synchronous signal which is in phase with an input signal comprising:

A/D conversion means for converting an input analog signal into a digital signal;

arithmetic means for generating a threshold which is used as a reference when the digital signal is binarized to generate a binarized signal and a synchronous clock for sampling the binarized clock, on the basis of the digital signal;

binarization means for comparing the digital signal with the threshold generated by the arithmetic means, and outputting a result of the comparison as a binarized signal; and

latch means for latching the binarized signal with the synchronous clock and outputting a PLL synchronous signal.

2. The digital PLL device of Claim 1 wherein

the arithmetic means comprise:

threshold detection means for detecting a maximum value and a minimum value of the digital signal in a predetermined period, and outputting an average of the maximum value and the minimum value as the threshold;

rise time detection means for detecting a rise time as a time of intersection of the threshold and a line connecting

two values of the digital signal, one of which is lower and the other of which is higher than the threshold, when the digital signal changes from the lower value to the higher value;

fall time detection means for detecting a fall time as a time of intersection of the threshold and a line connecting two values of the digital signal, one of which is higher and the other of which is lower than the threshold, when the digital signal changes from the higher value to the lower value;

input rate detection means for obtaining time intervals between the adjacent rise and the fall times during a predetermined period, and outputting a minimum value of the time intervals as an input rate of the analog signal; and

synchronous clock output means for obtaining a half timing of the input rate after an edge of the input analog signal is detected on the basis of the input rate and the rise and fall times and outputting a first one of the synchronous clock at that timing, and obtaining a timing of the input rate after the first synchronous clock is output and outputting a second or later one of the synchronous clock at that timing.

3. The digital PLL device of Claim 1 wherein the arithmetic means comprise:

threshold detection means for detecting integrals of the digital signal in a predetermined period, and outputting an average of the integrals as the threshold;

rise time detection means for detecting a rise time as a time of intersection of the threshold and a line connecting two values of the digital signal, one of which is lower and the other of which is higher than the threshold, when the digital signal changes from the lower value to the higher value;

fall time detection means for detecting a fall time as a time of intersection of the threshold and a line connecting two values of the digital signal, one of which is higher and the other of which is lower than the threshold, when the digital signal changes from the higher value to the lower value;

input rate detection means for obtaining time intervals between the adjacent rise and the fall times during a predetermined period, and outputting a minimum value of the time intervals as an input rate of the analog signal; and

synchronous clock output means for obtaining a half timing of the input rate after an edge of the input analog signal is detected on the basis of the input rate and the rise and fall times and outputting a first one of the synchronous clock at that timing, and obtaining a timing of the input rate after the first synchronous clock is output

and outputting a second or later one of the synchronous clock at that timing.

a 4. The digital PLL device of ~~any of~~ Claims 1 ~~to 3~~ comprising:

an oversampling digital filter for interpolating the adjacent digital signals.

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